THE ADVENT OF THE SIGNAL MICROPROCESSOR

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ABSTRACT

The Signal MicroProcessor [SMP] is a software controlled processor for analog RF and microwave signals which makes the implementation of new signal based systems practical much like the digital microprocessor did for data-based systems. The SMP is programmed using digital commands and processes analog RF and microwave signals without analog to digital conversion. The SMP, enabled by the ACT technology, is less complex and uses less power because it has the processing power of a multimillion transistor ASIC, but is implemented with less than 3000 transistors. The SMP is operated by a natural language software system.

INTRODUCTION

The Signal MicroProcessor (SMP) is a software-controlled processor for analog signals that gives designers the opportunity to take totally new approaches to the implementation of RF and microwave systems. In the past 15 years, the power of software-programmable data processing embodied in the digital microprocessor has revolutionized the telecommunication, personal computing, and electronic control industries. While these computational techniques are directly applicable to radars, spread-spectrum receivers, artificial intelligence, speech recognition and image processing, the digitization and computational requirements of such applications demand the use of high-speed analog to digital convertors (ADCs) and large, powerful computers operating in a non-realtime mode.

The SMP has been enabled by a new high-speed buffer memory technology called Acoustic Charge Transport (ACT). The ACT is a sample memory that converts input signals to packets of electrons with a quantity of charge proportional to the amplitude of the signal at the sampling time. Each packet of charge is isolated and transported by ultrasound from one processor to the next. The massively parallel architecture of the ACT computational engine has allowed multiply-and-accumulate times as low as 25 picoseconds to be realized.

Storing sample strength as a quantity of charge has several advantages over the conventional approach of encoding and storing information in the form of bits:

1. The problem of encoding wide-bandwidth signals with an ADC is eliminated or at least postponed until after initial processing has reduced the requirements on the ADC.

2. The multiplication process is greatly simplified because a signal stored in the form of an amplitude is multiplied by a coefficient simply by running it through a programmable attenuator. The attenuator output is the product of the digitally programmed attenuation times the signal. The programmable attenuator multiplies at rates exceeding 360 million samples per second, consumes practically no power and occupies a small fraction of the chip area required for a digital multiplier. Because of this reduction in complexity and power consumption, it becomes practical to implement hundreds or even thousands of multipliers on a single chip; each operating at rates exceeding several hundred million multiplies per second.

3. The accumulation process is greatly simplified when the product signal is represented by an amplitude because the summation is inherently accomplished by the buss that connects all the multipliers together. A summing buss accumulates samples at a rate exceeding 45 billion per second, consumes no power and occupies only the chip area required to make an electrical connection.

4. Transporting the sample from multiplier to multiplier with ultrasound is well-suited to FIR processing; this process reduces noise and greatly simplifies the controller and software required to coordinate the large number of parallel processors.

ENABLING TECHNOLOGY

The operation of the ACT delay line that acts as a buffer memory for the SMP processor is illustrated in Figure 1. The piezoelectric GaAs substrate is fitted with a transducer to generate a surface acoustic wave (SAW) which transports the information from one processor to the next. The SAW creates a travelling potential well that captures a packet of electrons at the source and transports it down the transport channel; the number of electrons in each packet is proportional to the voltage on the source at the sampling time. The SAW transports the subsurface packet down the channel to the drain at the opposite end without the aid of any surface features. Packets are sensed at any point along the propagation path by using a nondestructive sense electrode (NDS) across the clear surface of the transport channel and connecting it to a programmable attenuator multiplier.

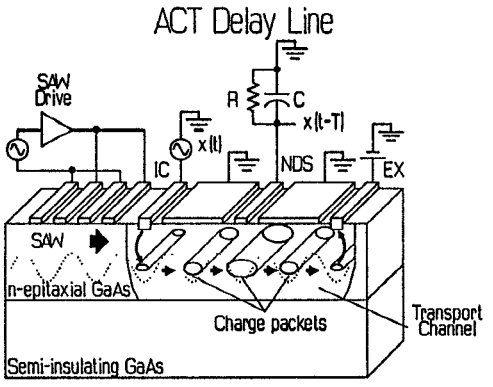

Figure 1

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Several points should be noted:

1. The sample memory tap or output port senses the charge but does not change the number of electrons in the packet. True nondestructive sensing is realized.

2. The absence of features above the transport channel leaves room for implementing the sample memory readout ports. These ports provide the inputs to the many multipliers (programmable attenuators) located along the channel.

3. Moving information from one processor to the next usually gives rise to system noise; the ultrasonic transport eliminates that noise.

4. The sampling rate of the ACT device typically runs from 200 MHz to 1 GHz and results in very high speed processors.

5. The ACT is implemented on semiconducting GaAs so that high speed attenuators, switches and digital RAM required to implement the SMP are monolithically constructed on the SMP substrate.

INITIAL EMBODIMENT

The first SMP is a 128-tap finite impulse response (FIR) filter with supporting electronics as shown in the schematic in Figure 2. It is implemented using 128 multipliers and accumulators along with the ACT sample memory on a single chip. The current implementation has an 8-bit by 5-bit multiplier accuracy, although the phase and amplitude stability of the SMP are sufficient to operate two units in parallel to achieve 8-bit by 8-bit accuracy. This SMP implements an FIR filter with a processing rate of 45 billion multiply-and-accumulate operations per second. The device is contained in a one-square-inch flatpack that dissipates less than 3 watts of power.

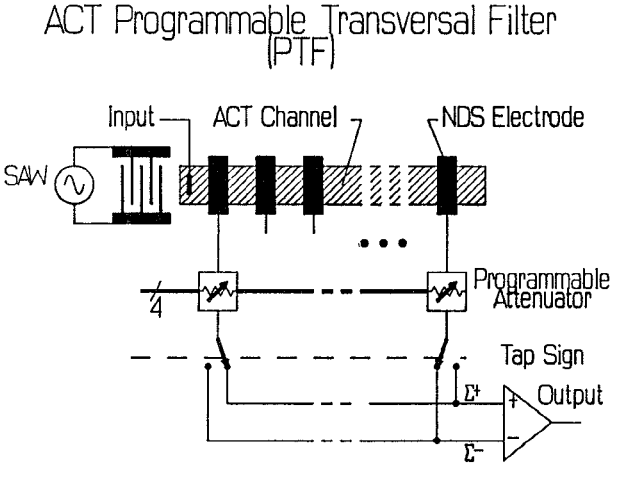


Figure 2

SMP DEVELOPMENT STATION

In order to demonstrate the potential of the SMP and to stimulate its application to RF and microwave systems, the concept of an SMP "development station" has been introduced. Development stations for digital processors generally supply all the hardware and software interfaces required to operate a processor with an existing computer. The SMP development station allows users to operate SMPs using only a personal computer (PC) running a single software program. Since some applications require more than one SMP, the development station is modular with a common digital and RF interface.

The SMP development station connects to a PC through a parallel port and is controlled by a signal processing and acquisition program called W.A.V.E.®. The SMP development station reduces engineering time because it is self-contained: a design may be theoretically modelled, the SMP programmed, the measured response acquired, and the accuracy of the model verified.

SMP APPLICATIONS

The SMP is more than a filter; it is able to perform the four basic signal processing functions of signal generation, extraction, modification, and characterization.

Signal generation: SMP-based direct digital synthesizers, signature generators, pulsers and frequency synthesizers are digitally controlled waveform generators with sampling rates exceeding 400 MHz.

Signal extraction: SMP-based matched filters, FIR filters, recursive filters and interference cancellers have digitally programmed responses. SMP-based channelizers separate signals into component frequencies and allow programmable selection on the basis of frequency.

Signal modification: SMP-based equalizers, step response shapers, target simulators and channel simulators operate on signals with 100-MHz bandwidths and are digitally programmable.

Signal characterization: SMP-based autocorrelators are used to measure signal statistics and the frequency of multipath and interference signals. SMP-based network analyzers measure impulse responses, transfer functions, impedance and time domain reflections. SMP-based pattern matchers identify signatures, measure time of arrival, characterize signals and perform transforms.

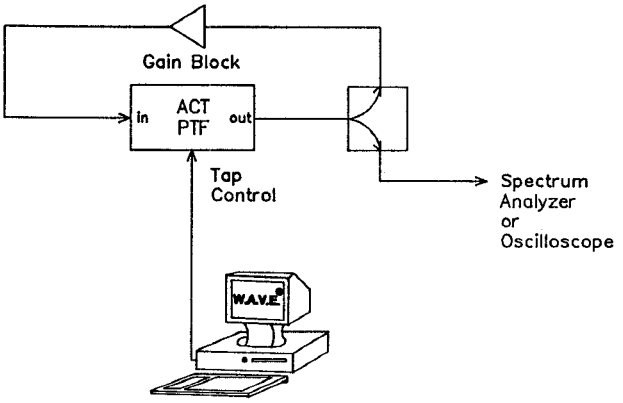
EXAMPLES OF SMP APPLICATIONS

The following 3 examples illustrate the utility and performance of the SMP.

Digitally Controlled Oscillator

Concept Description: The ACT digitally controlled oscillator (DCO) is a low-noise, low-complexity programmable frequency source. The DCO is implemented using the SMP as a delay-line oscillator. The output of the SMP is connected to the input with a loop gain greater than 1, causing the circuit to oscillate. The loop gain is made less than 1 at all frequencies away from the desired oscillation frequency by programming the SMP as a passband filter. The round-trip phase shift is 0 degrees at only one frequency, and that frequency may be selected by varying the delay of the SMP filter. A conceptual block diagram of the DCO is shown in Figure 3.

Results: The demonstration model of the DCO can shift relative frequencies by steps as small as 1 KHz over a range from 15 MHz to 85 MHz. It can be set to an absolute frequency with a precision of ± 2.5 KHz if module temperature is considered in the tap settings. Figure 4 shows the DCO output measured with 1-KHz resolution bandwidth; Figure 5 shows a 1 KHz per division superposition of the DCO output when it was programmed to 80.010 MHz and 80.011 MHz.



Digitally Controlled Oscillator Test Configuration

Figure 3

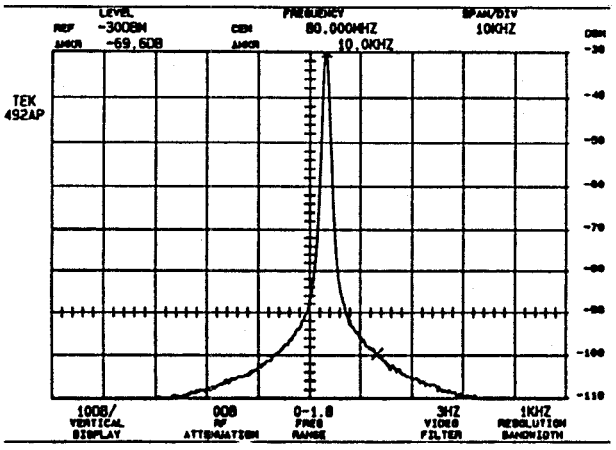


Figure 4

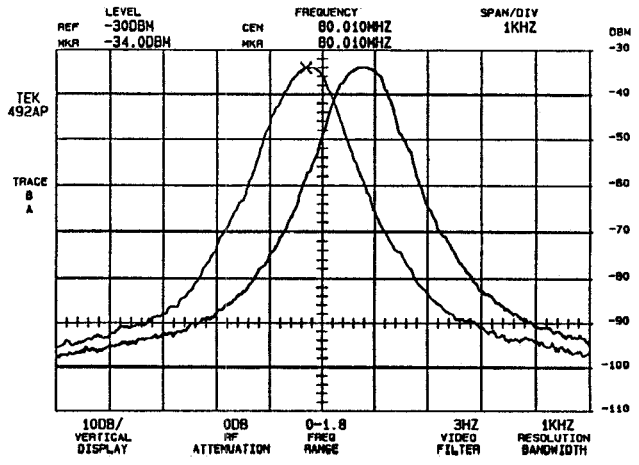


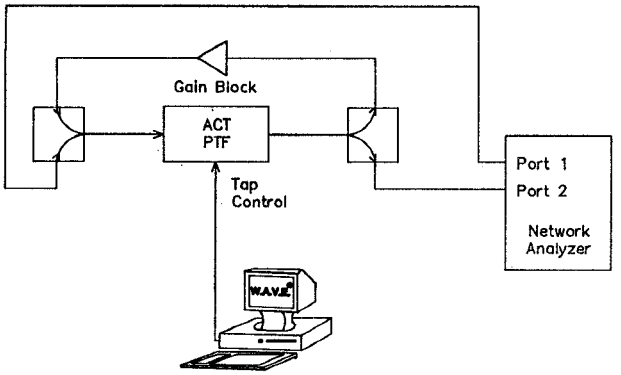
Figure 5

Programmable Narrowband Filter

Concept Description: The ACT programmable narrowband filter (PNF) is a two pole, high-Q filter with digitally selectable center frequency. The PNF is implemented using an SMP in a recursive filter mode as shwon in Figure 6. As in the oscillator described above, the output of the SMP is connected to the input. However, in the recursive filter mode, the loop gain is set to just under 1 at the center of the desired passband; the delay of the filter is adjusted to provide an open-loop phase shift of 0 degrees at the desired center frequency of the filter.

Results: The band narrowing of the recursive filter is illustrated in Figure 7, which shows the FIR response of the SMP used as a transversal filter superimposed on the recursive filter response.

The demonstration model of the PNF has programmable range from 15 MHz to 85 MHz; Figure 8 shows the superimposed PNF transfer functions as it is programmed from 20 MHz to 80 MHz. This model of the PNF can shift center frequencies by steps as small as several KHz.



Narrowband Filter Test Configuration

Figure 6

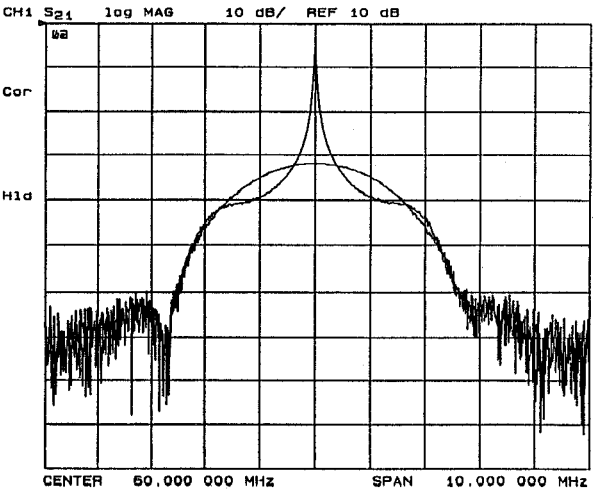


Figure 7

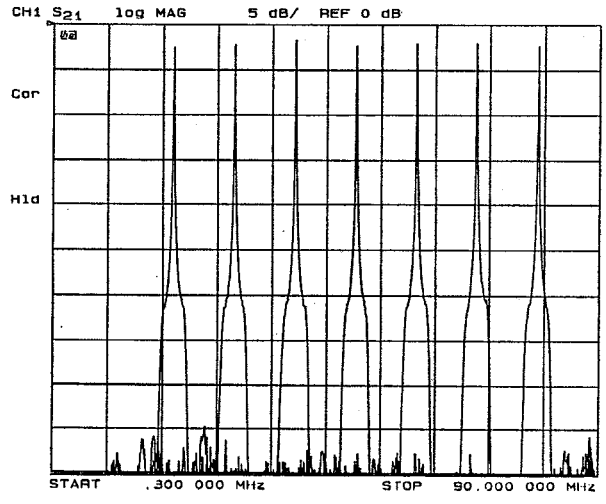
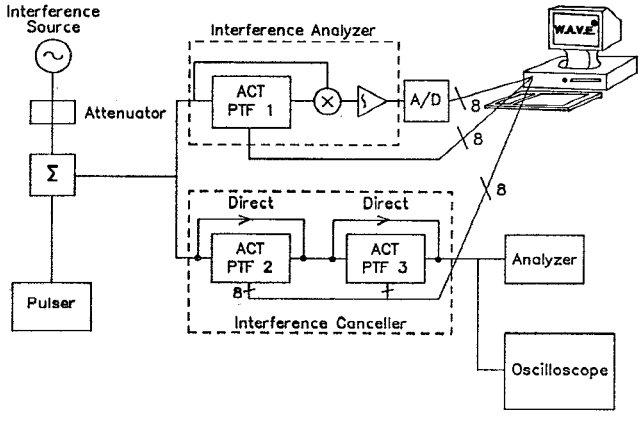


Figure 8

Interference Canceller

Concept Description: The SMP interference canceller is an adaptive filter that is designed to reduce the level of narrowband interference in wideband systems. It identifies the strongest interfering signal, precisely determines its frequency and produces a cancelling signal at that frequency to reduce interference with minimum perturbation to the wideband signal.

The interference canceller uses the SMP to measure the autocorrelation function of the signal-plus-interference waveform. The power density spectrum is then calculated to determine the precise frequency of the interference. Once this frequency is known, an SMP is programmed to produce a 180-degree phase shifted version of the interference which is used to cancel the unwanted signal. The system block diagram is shown in Figure 9.



Interference Canceller Test Configuration

Figure 9

Results: The ability to locate and cancel narrowband interference on a wideband signal is illustrated in Figure 10. Figures 10a and 10b show the time- and frequency-domain response of the system when an interference signal exists which is 30 dB stronger than the desired signal. When the SMP canceller is turned on, the desired signal (in this case a simple pulse) is clearly visible on the oscilloscope in Figure 10c, and the spectrum in Figure 10d is seen to be only slightly modified by the notch filter. Note that the notch reduces the interference level by approximately 60 dB.

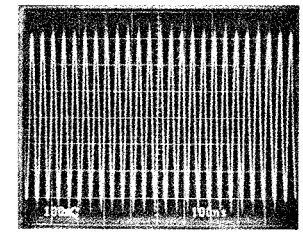


Figure 10a

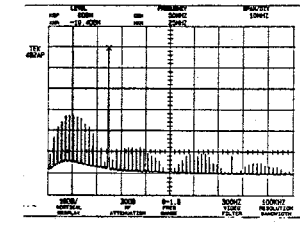


Figure 10b

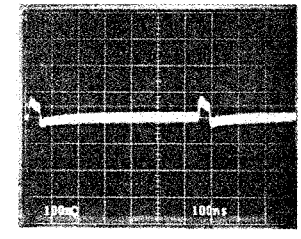


Figure 10c

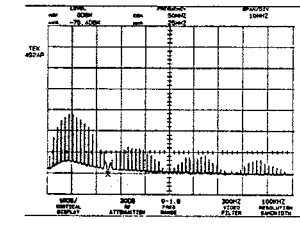


Figure 10d

IMPACT AND CONCLUSIONS

The SMP presents a unique challenge to designers working in the RF and microwave field; it has many of the features that made the digital microprocessor successful:

- Programmability: The SMP can be tailored to many applications with software, eliminating NRE costs.
- Development station support: Reduction in the engineering effort required to prototype a proposed system is made possible throughthe use of the SMP development station.
- Small size: The SMP is a small 5000-transistor chip that eliminates the need for high speed ADCs & DACs and performs the equivalent processing of a multimillion transistor ASIC.
- Price advantage of commonality: The SMP commonality allows each user to benefit from the volume of others.